Claims

[c1] A method for forming an etched pattern on a semiconductor substrate, the method comprising the steps of:
depositing a thin film on the substrate;
depositing a layer of planarizing material on the thin film;
depositing a layer of barrier material on the layer of planarizing material;
depositing at least one layer of imaging material on the layer of barrier material;
forming at least one first pattern shape in the layers of imaging material, barrier material and planarizing material;
removing the imaging material, either after or concurrently with forming the first pattern shape in the planarizing material;
transferring the first pattern shape to the thin film;
removing the barrier layer, either after or concurrently with transferring the first pattern shape to the thin film; and
removing the planarizing material.

[c2] The method of Claim 1, wherein at least one second pattern shape is formed in the thin film prior to depositing the layer of planarizing material, and the second pattern shape is filled by the planarizing material.

[c3] The method of Claim 1, wherein the thin film is a dielectric material.

[c4] The method of Claim 3, wherein the thin film is a low-k dielectric material.

[c5] The method of Claim 3, wherein the low-k dielectric material has a dielectric constant less than 3.9.

[c6] The method of Claim 3, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

[c7] The method of Claim 1, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9-anthracenylmethylated poly (hydroxystyrene), tetrahydro-1,3,4,6-tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and p-nitrobenzyl tosylate (pNBT).

[c8] The method of Claim 1, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

[c9] The method of Claim 1, wherein the barrier material comprises silicon dioxide deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100 degrees C to about 225 degrees C.

[c10] The method of Claim 9, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150Â°C.

[c11] The method of Claim 1, wherein the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride.

[c12] The method of Claim 1, further comprising the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the first pattern shape in the planarizing material.

[c13] The method of Claim 1, further comprising the step of filling the first pattern shape with a conductive material, after removing the imaging material, the barrier material and the planarizing material.

[c14] The method of Claim 13, wherein the conductive material comprises copper.

[c15] A method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of:
depositing a dielectric material on the substrate;
forming at least one via in said dielectric material, such that at least one of the vias is positioned over the patterned

conductor;

depositing a layer of planarizing material on the dielectric material and in the via;

depositing a layer of barrier material on the layer of planarizing material;

depositing at least one layer of imaging material on the layer of barrier material;

forming at least one trench in the layers of imaging material, barrier material and planarizing material, such that at least one of the trenches is positioned over the via;

removing the imaging material, either after or concurrently with forming the trench in the planarizing material;

transferring the at least one trench to the dielectric material, such that at least one of the trenches is positioned over the via;

removing the barrier material, either after or concurrently with transferring the at least one trench to the dielectric material; and

removing the planarizing material.

[c16] The method of Claim 15, wherein the dielectric material is a low-k dielectric material.

[c17] The method of Claim 16, wherein the low-k dielectric material has a dielectric constant less than 3.9.

[c18] The method of Claim 16, wherein the low-k dielectric material

has a dielectric constant less than about 3.2.

[c19] The method of Claim 16, wherein the low-k dielectric material is SiCOH deposited by chemical vapor deposition.

[c20] The method of Claim 15, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9-anthracenylmethylated poly (hydroxystyrene), tetrahydro-1,3,4,6-tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and p-nitrobenzyl tosylate (pNBT).

[c21] The method of Claim 20, further comprising the step of baking the planarizing material at a temperature of about 200Â°C to about 250Â°C, after deposition of the planarizing material.

[c22] The method of Claim 20, further comprising the step of baking the planarizing material at a temperature of about 225Â°C, after deposition of the planarizing material.

[c23] The method of Claim 15, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

[c24] The method of Claim 15, wherein the barrier material is silicon

dioxide.

[c25] The method of Claim 24, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100Â°C to about 225Â°C.

[c26] The method of Claim 24, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150Â°C.

[c27] The method of Claim 15, wherein the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and tantalum nitride.

[c28] The method of Claim 15, further comprising the steps of:
depositing a layer of anti-reflective coating on the barrier material, prior to deposition of the layer of imaging material; and
removing the anti-reflective coating, either after or concurrently with forming the trench in the planarizing material.

[c29] The method of Claim 15, further comprising the step of filling the via and the trench with a conductive material, after removing the imaging material, the barrier material and the planarizing material.

[c30] The method of Claim 29, wherein the conductive material

comprises copper.

[c31] The method of Claim 15, wherein the at least one via has a height, and the layer of planarizing material has a thickness of about half the via height to about twice the via height.

[c32] The method of Claim 15, wherein the layer of barrier material has a thickness of about 50 to 100 nm.

[c33] A method for forming a dual damascene interconnect structure on a semiconductor substrate comprising at least one patterned conductor, the method comprising the steps of:
depositing a dielectric material on the substrate;
forming at least one trench in the dielectric material, such that at least one of the trenches is positioned over the patterned conductor;
depositing a layer of planarizing material on the dielectric material and in the trench;
depositing a layer of barrier material on the layer of planarizing material;
depositing at least one layer of imaging material on the layer of barrier material;
forming at least one via in the layers of imaging material, barrier material and planarizing material, such that at least one of the vias is positioned over the trench and the patterned conductor;
removing the imaging material, either after or concurrently with

forming the via in the planarizing material;

transferring the at least one via to the dielectric material, such that at least one of the vias is positioned over the trench and the patterned conductor;

removing the barrier material, either after or concurrently with transferring the at least one via to the dielectric material; and

removing the planarizing material.

[c34] The method of Claim 33, wherein the dielectric material is a low-k dielectric material.

[c35] The method of Claim 34, wherein the low-k dielectric material has a dielectric constant less than 3.9.

[c36] The method of Claim 34, wherein the low-k dielectric material has a dielectric constant less than about 3.2.

[c37] The method of Claim 34, wherein the low-k dielectric material is SiCOH deposited by chemical vapor deposition.

[c38] The method of Claim 33, wherein the planarizing material is a poly(hydroxystyrene)-based system comprising poly(4-hydroxystyrene), 9-anthracenylmethylated poly (hydroxystyrene), tetrahydro-1,3,4,6-tetrakis(methoxymethyl)-imidazo[4,5-d] imidazole-2,5-(1H,3H)-dione, and p-nitrobenzyl tosylate (pNBT).

[c39] The method of Claim 38, further comprising the step of baking

the planarizing material at a temperature of about 200Â°C to about 250Â°C, after deposition of the planarizing material.

[c40] The method of Claim 33, further comprising the step of baking the planarizing material at a temperature of about 225Â°C, after deposition of the planarizing material.

[c41] The method of Claim 33, wherein the planarizing material is selected from the group consisting of polyarylsulfones, polyhydroxystyrene-based derivatives, polyimides, polyethers, polyarylenesulfides, polycarbonates, epoxies, epoxyacrylates, polyarylenes, polyarylenevinylenes, polyvinylcarbazole, cyclicolefins, and polyesters.

[c42] The method of Claim 33, wherein the barrier material is silicon dioxide.

[c43] The method of Claim 42, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 100Â°C to about 225Â°C.

[c44] The method of Claim 42, wherein the barrier material is deposited by plasma-enhanced chemical vapor deposition at a temperature of about 150Â°C.

[c45] The method of Claim 33, wherein the barrier material comprises a material selected from the group consisting of silicon, silicon nitride, silicon carbide, titanium nitride, and

tantalum nitride.

[c46] The method of Claim 33, further comprising the steps of: depositing a layer of anti-reflective coating on the barrier material, prior to depositing the layer of imaging material; and removing the anti-reflective coating, either after or concurrently with forming the via in the planarizing material.

[c47] The method of Claim 33, further comprising the step of filling the via and the trench with a conductive material, after removing the imaging material, the barrier material and the planarizing material.

[c48] The method of Claim 47, wherein the conductive material comprises copper.

[c49] The method of Claim 33, wherein the layer of barrier material has a thickness of about 50 to 100 nm.